AMENDMENTS TO THE DRAWINGS

In accordance with U.S. Patent and Trademark Office practice, proposed drawing changes as REPLACEMENT SHEETS are attached, wherein Applicant proposes to amend the drawings in the above-identified application as follows:

Please amend Figures 1-3 by including the legend -- BACKGROUND ART --.

No new matter has been added. Approval is earnestly requested.

REMARKS

This is in full and timely response to the Office Action dated August 1, 2007.

Claims 1-3 are currently pending in this application, with claims 1, 2 and 3 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Petition Under 37 C.F.R. §1.144

A Petition Under 37 C.F.R. §1.144 requesting review of a restriction requirement made the Office Action of May 16, 2007 is provided along with this Amendment.

Timely review and consideration of the Petition along with the rejoinder of the allegedly distinct inventions is respectfully requested.

Drawing objections

Page 2 of the Office Action includes objections to the drawings.

While not conceding the propriety of this objection and in order to advance the prosecution of the above-identified application, the drawings have been amended.

Withdrawal of these objections is respectfully requested.

Rejection under 35 U.S.C. §102

Page 3 of the Office Action indicates that claims 1-3 have been rejected under 35 U.S.C. §103 as allegedly being unpatentable over the alleged Applicants' Admitted Prior Art: Figures 1-3 of the specification as originally filed (AAPA) in view of European Patent Application No. EP 1 014 334 (Nakajima).

This rejection is traversed at least for the following reasons.

Claims 1-3 - Claim 1 is drawn to a latch for latching a latched result from an upstream sampling latch, the latch comprising:

a CMOS latch cell;

a power switch for connecting said CMOS latch cell to a power supply; and

an input switch disposed at an input of said CMOS latch cell;

wherein said power switch and said input switch are switched on and off complementarily in such a manner:

with said CMOS latch cell disconnected from said power supply, data to be latched is set on said CMOS latch cell, and

with said input of said CMOS latch cell disconnected from the upstream sampling latch, said power supply to said CMOS latch cell is switched on to level-shift the data set on said CMOS latch cell.

Claim 2 is drawn to a latch driving method for driving a latch comprising a CMOS latch cell either for latching a latched result from an upstream sampling latch, the latch driving method comprising the steps of:

with said CMOS latch cell disconnected from a power supply, connecting an input of said CMOS latch cell to the upstream sampling latch so as to set corresponding data on said CMOS latch cell; and

with said input of said CMOS latch cell disconnected from said upstream sampling latch, switching on said power supply to said CMOS latch cell so as to level-shift the data set on said CMOS latch cell.

Claim 3 is drawn to a flat display apparatus comprising a display unit with pixels disposed in a matrix, and driving circuits for driving pixels of said display unit, said display unit and said driving circuits being formed integrally on a substrate;

wherein said driving circuits include a horizontal driving circuit for setting gradations for said pixels of said display unit, said horizontal driving circuit including:

a sampling latch for successively latching continuous video data;

a second latch for latching a latched result from said sampling latch on a line-by-line basis; and

a digital-to-analog converter circuit for converting an output of said second latch from digital to analog form for output to said display unit; and

wherein either said sampling latch or said second latch acts in such a manner:

with a CMOS latch cell disconnected from a power supply, an input of said CMOS latch cell is connected to the upstream sampling latch so as to set corresponding data on said CMOS latch cell, and

with said input of said CMOS latch cell disconnected from said upstream sampling latch, said power supply to said CMOS latch cell is switched on to level-shift the data set on said CMOS latch cell.

Figure 6 of the specification as originally filed is provided hereinbelow.

FIG. 6

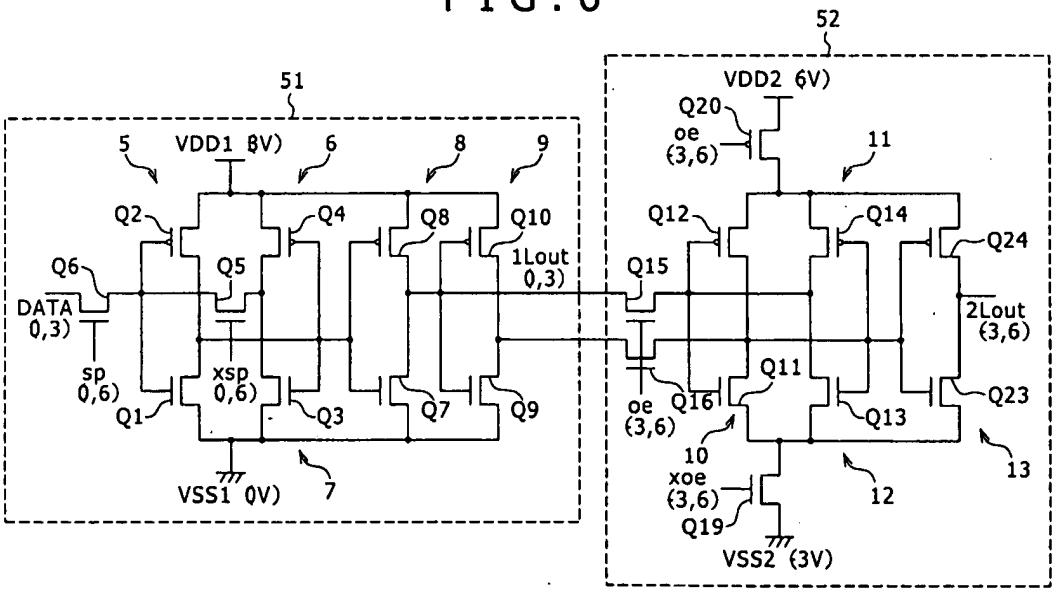
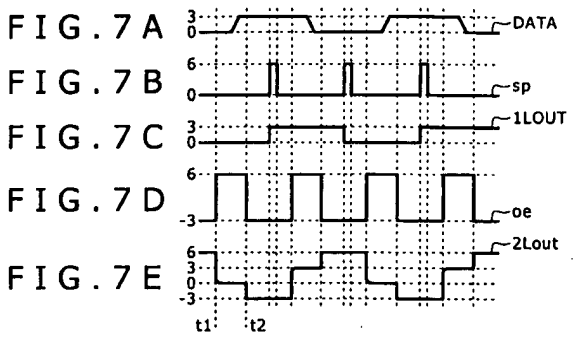


Figure 7 of the specification as originally filed is provided hereinbelow.



Paragraph [0039] of U.S. Patent Application Publication No. 2006/0055652, the publication document for the above-identified application, provides that:

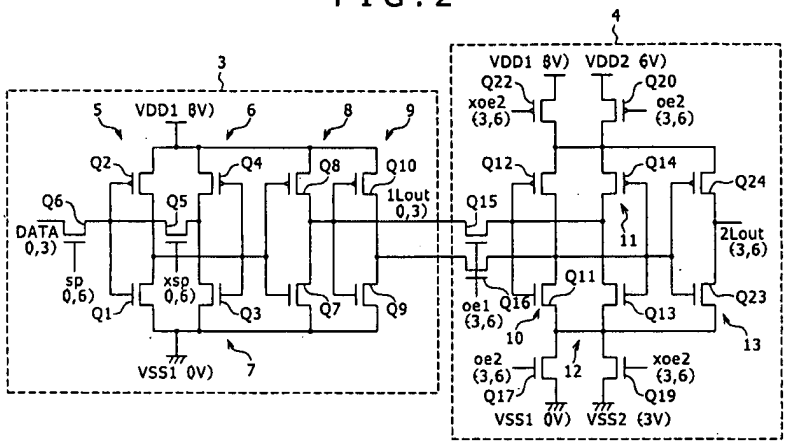
> In the second latch 52, *an output enable pulse "oe"* (FIG. 7D) having an amplitude of -3 to 6 V rises at a time t1. This causes the latched result 1Lout (FIG. 7C) from the sampling latch 51 to be transferred to the gates of the transistors Q11 through Q14 making up the CMOS inverters 10 and 11 (FIG. 7E). When the output enable pulse "oe" subsequently falls at a time t2, the second latch 52 is disconnected from the sampling latch 51 and the CMOS latch cell 12 is connected to the power supply VDD2. This allows a level-shifted data signal 2Lout to be output.

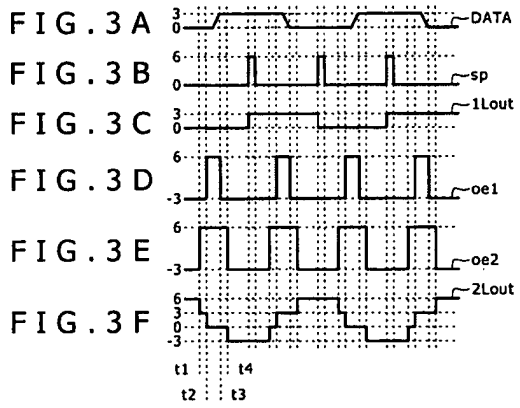
AAPA - Paragraph [0037] of U.S. Patent Application Publication No. 2006/0055652, the publication document for the above-identified application, provides that:

> The sampling latch 51, as shown in FIG. 6, has the *same structure* as that of the sampling latch 3 described above with reference to FIG. 2. The second latch 52, meanwhile, has basically the *same structure* as that of the conventional second latch 4 described above with reference to FIG. 2, ***except that*** the *transistors Q22 and Q17 disposed at the power supply and the ground respectively are* ***removed*** and that the *transistors Q19 and Q20 are* ***commonly controlled*** *by use of an output enable signal "oe"* for control over the input of the second latch 52.

Figures 2 and 3 of the specification as originally filed is provided hereinbelow.

FIG. 2





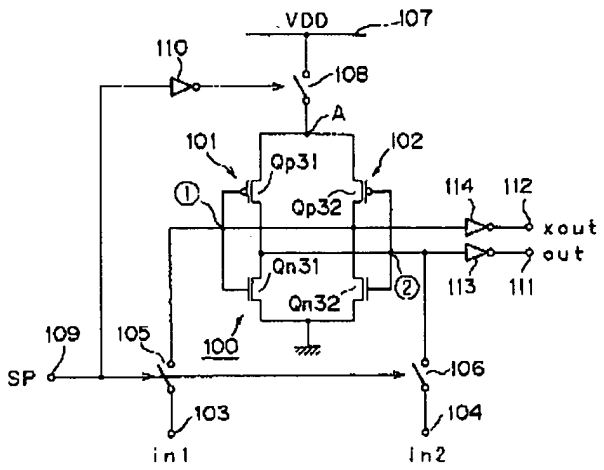
Moreover, a review of Figures 3D and 3E reveal that the output enable signal "oe1" ***is not a complement*** of the output enable signal "oe2".

Thus, AAPA fails to disclose, teach, or suggest that with a second latch (4) disconnected from a power supply (VDD1, VDD2, VSS1, VSS2), an input of second latch (4) is connected to the upstream sampling latch (3) so as to set corresponding data on the second latch (4); and with the input of the second latch (4) disconnected from the upstream sampling latch (3), the power supply

(VDD1, VDD2, VSS1, VSS2) is switched on to the second latch (4) so as to level-shift the data set on the second latch (4).

Nakajima - The Office Action cites Nakajima. In this regard, Figure 18 of Nakajima is provided hereinbelow.

FIG. 18



Paragraph [0177] of Nakajima arguably teaches a circuit diagram showing the sampling latch circuit of the first embodiment is shown in Fig. 18.

However, the Office Action ***fails*** to show within Nakajima that with the sampling latch circuit of the first embodiment being disconnected from a power supply (VDD), an input of the sampling latch circuit of the first embodiment is connected to an upstream sampling latch so as to set corresponding data on the sampling latch circuit of the first embodiment; and with the input of the sampling latch circuit of the first embodiment disconnected from the upstream sampling latch, the power supply (VDD) is switched on to the sampling latch circuit of the first embodiment so as to level-shift the data set on the sampling latch circuit of the first embodiment.

Withdrawal of this rejection and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Fees

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: December 28, 2007

Respectfully submitted,

By_____
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Attachments

REPLACEMENT SHEET